In the foregoing embodiments, the present invention has been described in case it is applied to the leadframe for fabricating the QFP, but can also be applied generally to the leadframes to be used for assembling the surface-mounting LSI package. The present invention can also be applied to a leadframe to be used for fabricating a pin-inserted LSI package such as DIP (i.e., Dual In-line Package).

The effects to be achieved by the representatives of the invention disclosed herein will be briefly summarized in the following:

(1) According to the present invention, it is possible to provide an LSI package having an improved reflow cracking resistance; and

(2) According to the present invention, a leadframe matching the flexible manufacturing system of the LSI package can be provided to reduce the production cost of the LSI package.

What is claimed is:

1. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip;

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mounting portion of said leadframe are continuously formed in an area of said semiconductor chip.

2. A semiconductor integrated circuit device according to claim 1, wherein each of said suspension leads includes a first portion and a second portion which is wider than said first portion, wherein said second portion is separated from said chip mounting portion and is positioned under said peripheral portion of said semiconductor chip, and wherein said semiconductor chip is fixed at said second portion of each of said suspension leads.

3. A semiconductor integrated circuit device according to claim 1, wherein said semiconductor chip is of a tetragonal shape.

4. A semiconductor integrated circuit device according to claim 1, wherein said semiconductor chip includes a rear surface opposing said main surface and is fixed to said chip mounting portion and said suspension leads at one portion of said rear surface, and wherein the other portion of said rear surface which is exposed from said chip mounting portion and said suspension leads is directly contacted to said resin member.

5. A semiconductor integrated circuit device according to claim 2, wherein said semiconductor chip is a rectangular shape and said suspension leads include four suspension leads, and wherein four corners of said rectangular-shaped semiconductor chip are supported by said four suspension leads.

6. A semiconductor integrated circuit device according to claim 5, wherein said resin member has a rectangular shape, and wherein said outer lead portions are extended outwardly from four sides of said rectangular-shaped resin member.

7. A semiconductor integrated circuit device according to claim 6, further comprising:

a plurality of grooves for positioning the semiconductor chip, said grooves each formed on said four suspension leads.

8. A semiconductor integrated circuit device according to claim 6, further comprising:

a plurality of projections for positioning the semiconductor chip, said projections each formed on said four suspension leads.

9. A semiconductor integrated circuit device according to claim 7, wherein said grooves are arranged on said four suspension leads so as to accord to four corners of said rectangular-shaped semiconductor chip.

10. A semiconductor integrated circuit device according to claim 8, wherein said projections are arranged on said four suspension leads so as to accord to four corners of said rectangular-shaped semiconductor chip.

11. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other and wherein said suspension leads and said chip mount-

ing portion of said leadframe are continuously formed in an area of said semiconductor chip.

12. A semiconductor integrated circuit device according to claim 11, wherein said semiconductor chip includes a rear surface opposing said main surface and is fixed to said chip mounting portion and said suspension leads at one portion of said rear surface, and wherein the other portion of said rear surface which is exposed from said chip mounting portion and said suspension leads is directly contacted to said resin member.

13. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a chip mounting portion for mounting said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said chip mounting portion is smaller than said semiconductor chip and is positioned under a substantially central portion of said semiconductor chip, said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and

an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.

14. A semiconductor integrated circuit device comprising:

a semiconductor chip having a main surface including semiconductor elements and a plurality of bonding pads;

a leadframe having:

a cracking suppression means for mounting said semiconductor chip thereon and for suppressing, during a reflow soldering processing, device cracking, wherein said cracking suppression means is a chip mounting portion which is smaller than said semiconductor chip and which is positioned under a substantially central portion of said semiconductor chip,

suspension leads unitarily formed with said chip mounting portion, a width of said chip mounting portion being wider than a width of each of said suspension leads,

a plurality of inner lead portions arranged to surround said semiconductor chip and being electrically connected with said bonding pads by bonding wires, and

a plurality of outer lead portions individually connected with said inner lead portions; and

a resin member sealing said semiconductor chip, said inner lead portions, said chip mounting portion, said suspension leads and said bonding wires;

wherein said semiconductor chip is fixed to said chip mounting portion by adhesive, said semiconductor chip is fixed to a part of each of said suspension leads by adhesive which is located under a peripheral portion of said semiconductor chip, and an adhesive region of said chip mounting portion and said semiconductor chip and an adhesive region of each of said suspension leads and said semiconductor chip are separated from each other.